

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +30V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for $\pm 10V$ switch driver applications. Other characteristics allow them to be used as $\pm 5V$ switches. The SD214 and 215 are designed to switch signals up to $\pm 10V$ and the SD212 and 213 are designed to switch signals up to $\pm 5V$.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

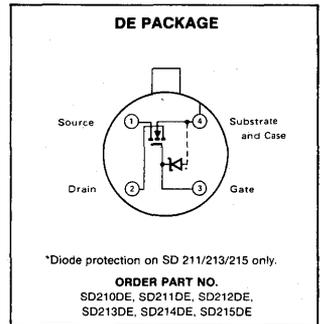
FEATURES

- Low feedback capacitance: 0.30pF
- Low drain node capacitance: 1.3pF
- Low gate node capacitance: 2.4pF
- Low feedthrough and feedback transients
- Ion-implanted for greater reliability
- Excellent isolation from input to output: -120dB
- 35V drain-to-source voltage for SD210/211
- Military qualifications pending

APPLICATIONS

- Switch driver
- Analog switch
- Multiplexers
- Digital switch
- Sample and hold
- Choppers
- A-TO-D converters
- D-TO-A converters

PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (all devices)

PARAMETER	RATING	UNIT
Drain current (I _D)	50	mA
Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
Transistor dissipation (P _T)		
At 25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At 25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.*

PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNIT
V _{DS} Drain-to-source	+30	+30	+10	+10	+20	+20	Vdc
V _{SD} Source-to-drain*	+10	+10	+10	+10	+20	+20	Vdc
V _{DB} Drain-to-substrate	+30	+30	+15	+15	+25	+25	Vdc
V _{SB} Source-to-substrate	+15	+15	+15	+15	+25	+25	Vdc
V _{GS} Gate-to-source	±40	-15	±40	-15	±40	-25	Vdc
V _{GB} Gate-to-substrate	±40	+25	±40	+25	±40	+30	Vdc
V _{GD} Gate-to-drain	±40	-0.3	±40	-0.3	±40	-0.3	Vdc
		+25		+25		+30	
		+25		+25		+30	

*NOTE

Refer to test conditions specified in Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD210			SD211			SD212			UNIT		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
Breakdown voltage													
BV _{DS}	Drain-to-source	V _{GS} = V _{BS} = 0V, I _D = 10 μ A		30	35		30	35				V	
		V _{GS} = V _{BS} = -5V, I _S = 10nA		10	25		10	25		10	25	V	
BV _{SD}	Source-to-drain	V _{GD} = V _{BD} = -5V I _D = 10nA		10			10			10		V	
BV _{DB}	Drain-to-substrate	V _{GB} = 0V, source OPEN I _D = 10nA		15			15			15		V	
BV _{SB}	Source-to-substrate	V _{GB} = 0V, drain OPEN I _S = 10 μ A		15			15			15		V	
Leakage current													
I _{DS} (OFF)	Drain-to-source	V _{GS} = V _{BS} = -5V V _{DS} = +10V			1	10		1	10		1	10	nA
I _{SD} (OFF)	Source-to-drain	V _{GD} = V _{BD} = -5V V _{SD} = +10V			1	10		1	10		1	10	nA
I _{GS}	Gate	V _{DB} = V _{SB} = 0V V _{GB} = \pm 40V V _{GB} = +25V				0.1			10			0.1	nA μ A
V _T	Threshold voltage	V _{DS} = V _{GS} = V _T , I _S = 1 μ A V _{SB} = 0V		0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	V
r _{DS} (ON)	Drain-to-source resistance	I _D = 1.0mA, V _{SB} = 0 V _{GS} = +5V V _{GS} = +10V V _{GS} = +15V V _{GS} = +20V V _{GS} = +25V			50 30 23 19 17	70 45		50 30 23 19	70 45		50 30 23 19 17	70 45	Ω Ω Ω Ω Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SD213			SD214			SD215			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage											
BV _{DS} Drain-to-source	$V_{GS} = V_{BS} = -5V, I_S = 10nA$	10	25		20	25		20	25		V
BV _{SD} Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			20			20			V
BV _{DB} Drain-to-substrate	$V_{GB} = 0V, \text{source OPEN}$ $I_D = 10nA$	15			25			25			V
BV _{SB} Source-to-substrate	$V_{GB} = 0V, \text{drain OPEN}$ $I_S = 10\mu A$	15			25			25			V
Leakage current											
I _{DS(OFF)} Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$ $V_{DS} = +20V$		1	10							nA
I _{SD(OFF)} Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$ $V_{SD} = +20V$			1		10		1	10		nA
I _{GBS} Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$ $V_{GB} = +25V$ $V_{GB} = +30V$			10					0.1		nA μA μA
V _T Threshold voltage	$V_{DS} = V_{GS} = V_T, I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
r _{DS(ON)} Drain-to-source resistance	$I_D = 1.0mA, V_{SB} = 0$ $V_{GS} = +5V$ $V_{GS} = +10V$ $V_{GS} = +15V$ $V_{GS} = +20V$ $V_{GS} = +25V$		50 30 23 19	70 45		50 30 23 19 17	70 45		50 30 23 19 17		Ω Ω Ω Ω Ω

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

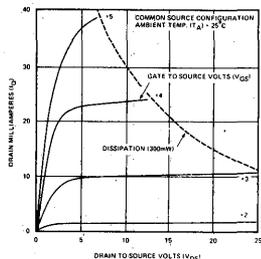
PARAMETER	TEST CONDITIONS	SD210			SD211			SD212			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
g _{fs} Forward transconductance	$V_{DS} = 10V, V_{SB} = 0V$ $I_D = 20mA, f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)											
	$V_{DS} = 10V, f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
C _(GS+GD+GB) Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
C _(GD+DB) Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
C _(GS+SB) Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C _{DG} Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$ unless otherwise specified.

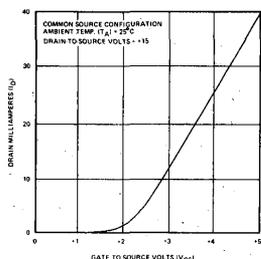
PARAMETER	TEST CONDITIONS	SD213			SD214			SD215			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
g _{fs} Forward transconductance	$V_{DS} = 10V, V_{SB} = 0V$ $I_D = 20mA, f = 1kHz$	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)											
	$V_{DS} = 10V, f = 1MHz$ $V_{GS} = V_{BS} = -15V$										
C _(GS+GD+GB) Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
C _(GD+DB) Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
C _(GS+SB) Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C _{DG} Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

TYPICAL PERFORMANCE CHARACTERISTICS

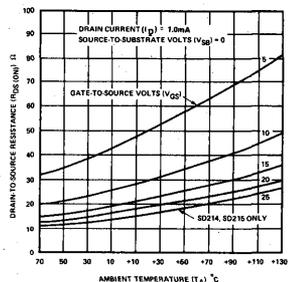
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



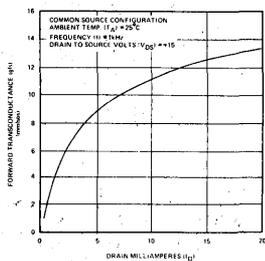
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



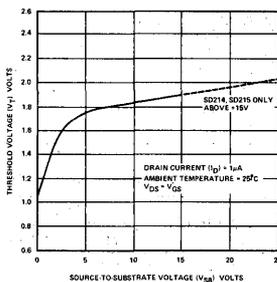
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



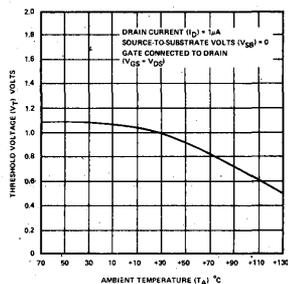
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



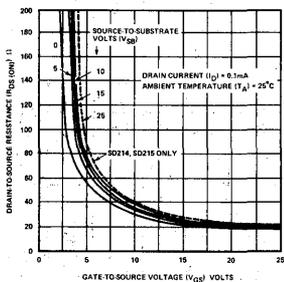
THRESHOLD VOLTAGE vs SOURCE-TO-SUBSTRATE VOLTAGE



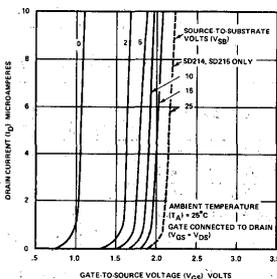
THRESHOLD VOLTAGE vs TEMPERATURE



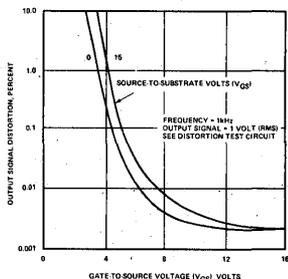
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



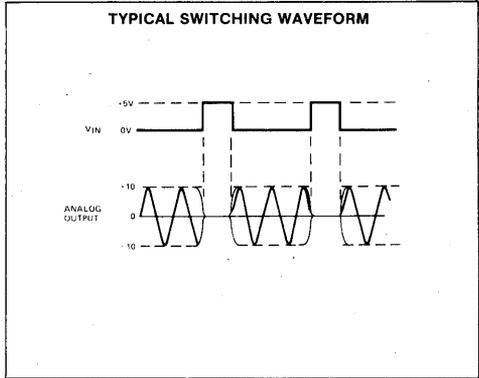
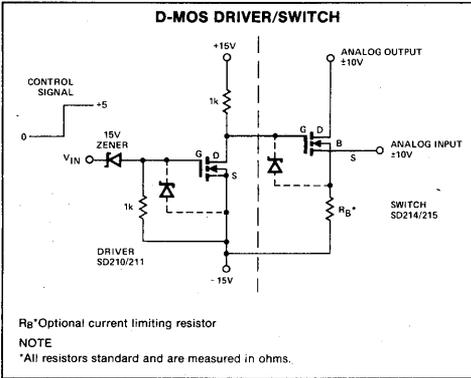
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



DISTORTION vs GATE-TO-SOURCE VOLTAGE



TYPICAL APPLICATION



TEST CIRCUITS

