ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 — Standard Conditions: V_{CC} = +5.0V, T = +25°C)

305, 306

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
"1" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$	0.15			V	I_{OUT} = –1.8 mA, V_{IN} = +3.8V
"0" OFFSET VOLTAGE	$V_{IN} - V_{OUT}$			–0.3	V	V_{IN} = +0.6V
"0" INPUT CURRENT	I_{IN}			–2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			6.0		mW	Each gate; 50% duty cycle
AVERAGE GATE DELAY (Measured at 50% points)	t_{pd}		15		ns	R_L = 16K to Gnd; C_L = 8 pF to Gnd; F.O. = 1
	t_{pd}		35		ns	R_L = 1.6K to Gnd; C_L = 75 pF to Gnd; F.O. = 10
FAN-OUT (To source loads)				10		Note 6

333, 314, 317, 370 and 380

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"		800	1200		mV	Note 8
NOISE IMMUNITY FOR "1"		1100	1700		mV	Note 8
"1" OUTPUT VOLTAGE						
(314, 317, 370, 380)	V_{OUT}	3.8			V	I_{OUT} = –2 mA, V_{IN} = +1.4V
(333 only))	V_{OUT}	3.8			V	I_{OUT} = –2 mA, V_{IN} = +2.7V
"0" OUTPUT VOLTAGE						
(314, 317, 370, 380)	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA, V_{IN} = +2.7V
(333 only)	V_{OUT}			0.6	V	I_{OUT} = 12.5 mA, V_{IN} = +1.4V
"1" INPUT CURRENT	I_{IN}			180	μA	V_{IN} = +2.7V
EXPANDER NODE VOLTAGE (317, 333)	V_N	1.85			V	V_{IN} = +2.7V
AVERAGE POWER CONSUMPTION (314, 317, 370, 380)			22		mW	Each gate; 50% duty cycle
(333 only)			44		mW	Each gate; 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		20		ns	7-stage ring oscillator
(314, 317, 370, 380)	t_{pd}		30		ns	7-stage ring oscillator, C_L = 130 pF/gate
AVERAGE GATE DELAY	t_d		20		ns	R_L = 16K to Gnd; C_L = 8 pF to Gnd; F.O. = 1
(333 at 50% points)	t_d		35		ns	R_L = 1.6K to Gnd; C_L = 130 pF to Gnd; F.O. = 12
FAN-OUT						
To sink loads				5		Note 6, 7
To source loads				11		Note 6, 7

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 5 – Standard Conditions: V_{CC} = +5.0V, T = +25°C)

356

CHARACTERISTIC	MEASUREMENT	MIN.	TYP.	MAX.	UNITS	CONDITIONS
NOISE IMMUNITY FOR "0"			800		mV	Note 8
NOISE IMMUNITY FOR "1"			1500		mV	Note 8
"1" OUTPUT VOLTAGE	V_{OUT}	3.5			V	I_{OUT} = –2 mA, V_{IN} = +1.0V
"0" OUTPUT VOLTAGE	V_{OUT}			0.6	V	I_{OUT} = 44 mA, V_{IN} = +2.7V
"0" INPUT CURRENT	I_{IN}			–2.5	mA	V_{IN} = +0.6V
AVERAGE POWER CONSUMPTION			37		mW	Each gate, 50% duty cycle
AVERAGE PROPAGATION DELAY	t_{pd}		55		ns	
FAN-OUT						
To sink loads				17		Note 6, 7
To source loads				11		Note 6, 7

Notes:

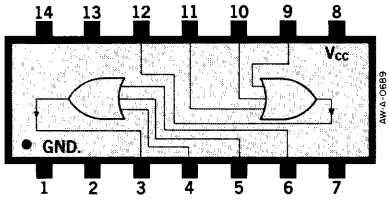
1. Pins not specifically referenced are left electrically open.
2. All voltage measurements are referenced to the ground pin. Positive current flow is defined as into the terminal indicated.
3. Maximum ratings are values above which serviceability may be impaired.
4. Precautionary measures should be taken to ensure current limiting per the maximum ratings should the isolation diodes become forward biased.
5. Positive Logic Definition: "UP" Level = "1"; "DOWN" Level = "0".
6. Sink load is defined as a 306 Input, source load is defined as a 317 Input.
7. This device is capable of accommodating the maximum specified sink and source loads concurrently.
8. This characteristic guaranteed by output voltage measurements.
9. Manufacturer reserves right to make design and process improvements.

NORMALIZED LOADING CHART (Notes 2 and 3)

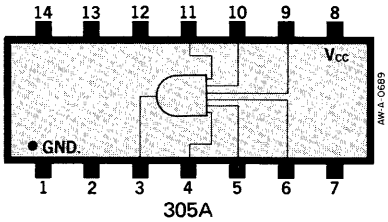
ELEMENT	INPUT LOAD		FAN-OUT		ELEMENT	INPUT LOAD		FAN-OUT	
	SINK	SOURCE	SINK	SOURCE		SINK	SOURCE	SINK	SOURCE
300		1.0	Note 1	Note 1	321, 322	N/A	N/A	5	8
305, 306	1.0			10	J,K INPUTS	0.7	0.5	N/A	N/A
314, 317		1.0	5	11	CLOCK, R_D (321)	2.5	1.0	N/A	N/A
370, 380		1.0	5	11	CLOCK' R_D (322)	1.3	0.5	N/A	N/A
333		1.0	5	11	S_D (321, 322)	1.3	0.5	N/A	N/A
356	1.0		17	11					

Loading Chart Notes:

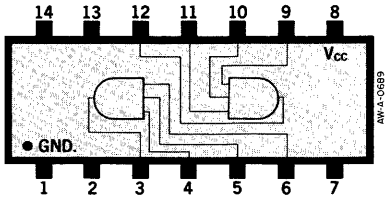
1. Output to connect to 317 or 333 expansion node only.
2. Normalized sink load is 306 maximum input current = -2.5 mA.
3. Normalized source load is 317 maximum input current = 180 μA.



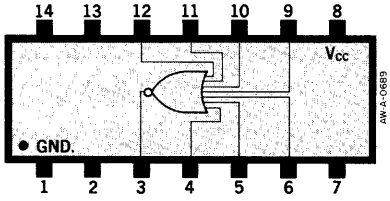
300A
DUAL 3-INPUT EXPANDER



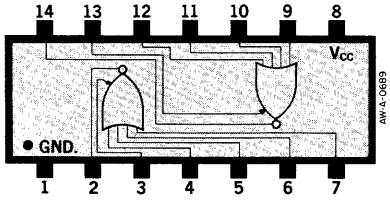
305A
6-INPUT AND GATE



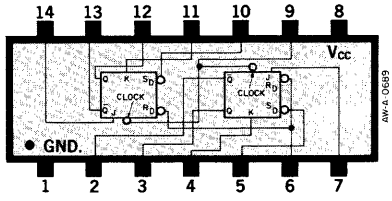
306A
DUAL 3-INPUT AND GATE



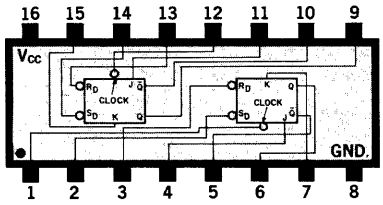
314A
7-INPUT NOR GATE



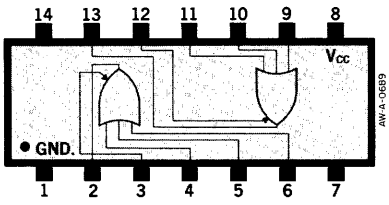
317A
DUAL 4-INPUT EXPANDABLE NOR GATE



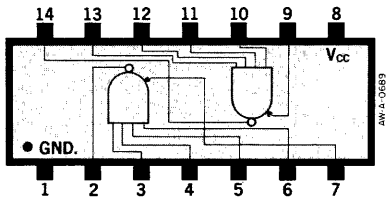
321A
DUAL J-K BINARY



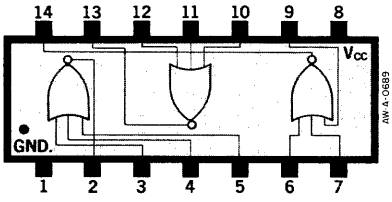
322B
DUAL J-K BINARY



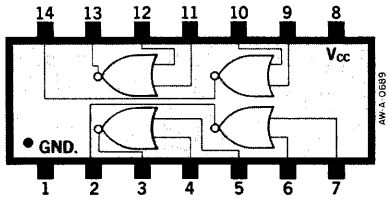
333A
DUAL 3-INPUT EXPANDABLE OR GATE



356A
DUAL 4-INPUT EXPANDABLE LINE DRIVER

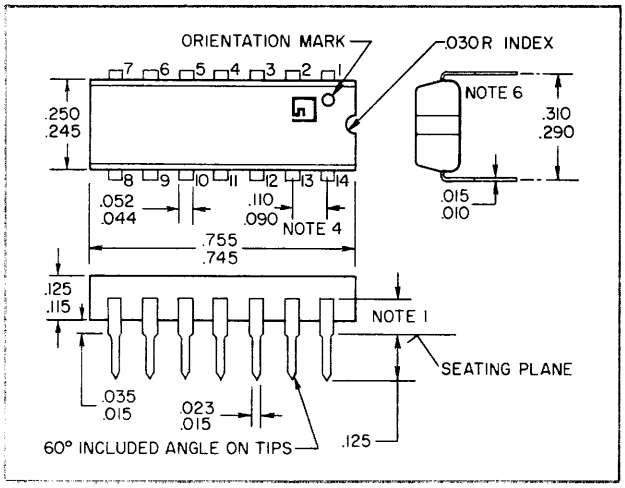


370A
TRIPLE 3-INPUT NOR GATE

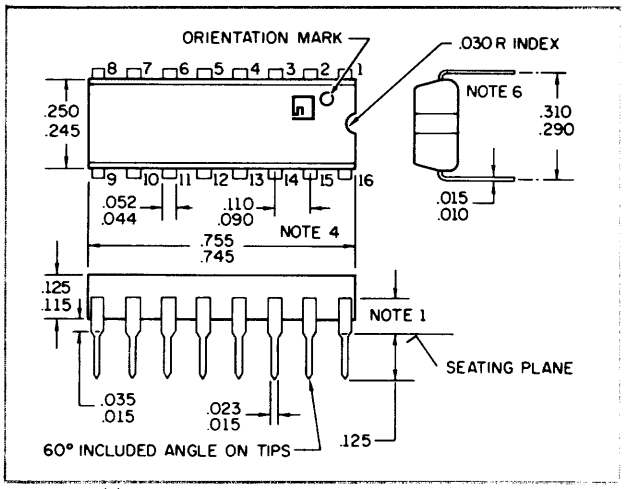


380A
QUAD 2-INPUT NOR GATE

A-PACKAGE



B-PACKAGE



NOTES:
(1) Lead spacing shall be measured within this zone.
(2) Molded Plastic Body.
(3) Kovar Leads.
(4) Lead spacing tolerances are non-cumulative.
(5) Thermal resistance from junction to still air, $\Theta_{J\text{-}A}$ = 0.16°C/mW.
(6) Leads shown as positioned by Signetics dual in-line package carrier.
(7) All dimensions of plastic package exclude molding-caused flash.

UTILOGIC II CIRCUITS

UTILOGIC II inputs are classified as sink loads and source loads by the direction of current flow required to activate the input. The input of the OR and NOR gates are called source loads because they must be driven by a source of current, e.g., the output of a UTILOGIC II element in the "1" state or a connection to the positive supply. The inputs of the AND gates and the Binary are called sink loads because they must be driven from a current sink; for example, the output of a UTILOGIC II element in the "0" state or a connection to ground.

In this publication, and all other UTILOGIC II literature, the convention of positive logic, i.e., the positive level is "1", has been assumed. If the negative logic notation is assumed (most negative level is "1"), the AND, OR, and NOR gates become OR, AND, and NAND respectively.

The characteristic curves presented in the various sections are designed to allow the system designer to predict system performance characteristics for various operating conditions. In general, characteristics are normalized to the conditions of the specification sheets. The use of the normalized characteristic is a definite design aid in that it is usually the change in the characteristic as a result of a change in the parameter that is of interest.

As long as the effects, e.g., $\frac{\partial V_{sat}}{\partial Temp.}$, are small, the total effect may be predicted by taking the product of the individual effects.

Throughout the discussion that follows, V_{CC} is assumed to be 5.0V unless otherwise specified.

UTILOGIC II AND Gates

The UTILOGIC II AND gates 305 and 306 are fabricated from the same basic chip, and therefore have identical electrical characteristics. The internal connection pattern is varied to produce a single 6-input AND gate in the 305, and the dual 3-input AND gates in the 306.

CIRCUIT DESCRIPTION

Schematic diagrams of the UTILOGIC II AND gates are shown in Figures 1 and 2. The multiple-emitter input structure provides the same function as a Diode AND gate. The output-emitter follower provides the current gain necessary for high fan-out, and also reduces the offset voltage associated with Diode AND gates. The emitter follower provides a low output impedance to effect fast response on "0" to "1" transitions and the current gain necessary for source current fan-out. The input transistor and connecting diode provide a low impedance circuit to maintain good response on "1" to "0" transitions.

Input Characteristics

The input of the AND is defined as a standard UTILOGIC II sink load. The standard sink load may be simulated by 2 kohm resistor with a series diode to the supply voltage. The input impedance of UTILOGIC II AND gates

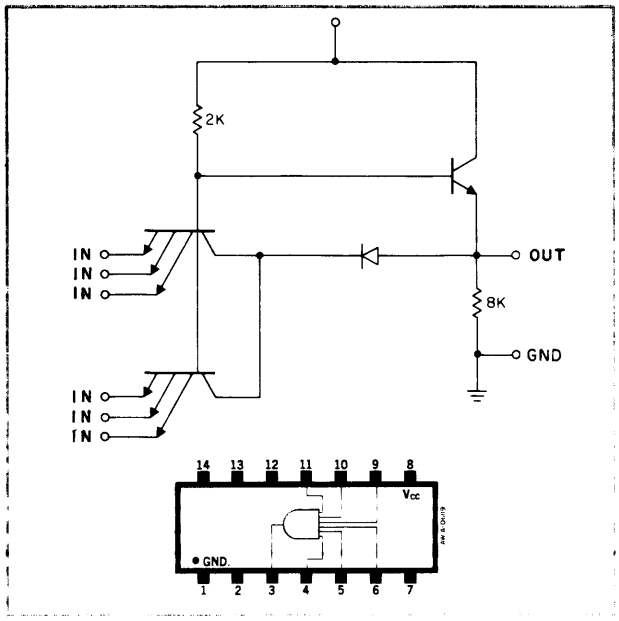


Figure 1 305 6-Input AND Gate

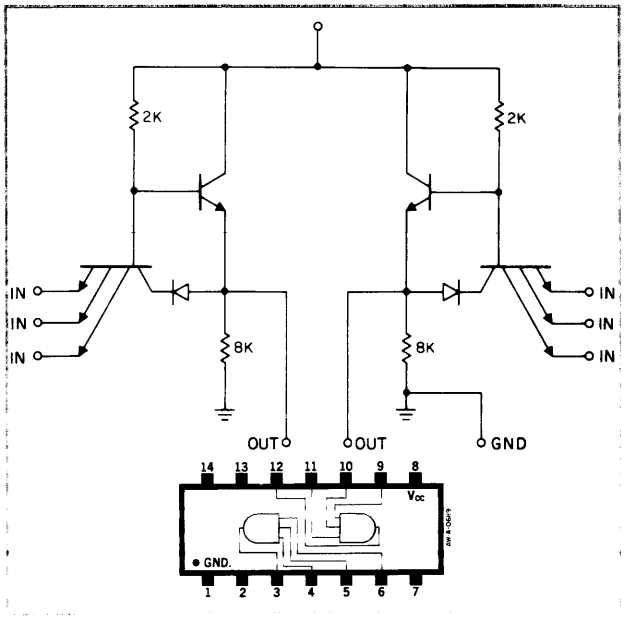


Figure 2 306 Dual 3-Input AND Gate

is low enough so that unused inputs may be left open without degrading circuit performance (open inputs are logical "1") however; it is recommended that unused inputs be connected to the used inputs of the circuit. Connecting the unused inputs to used inputs of the same circuit will not increase the circuit loading. The effect of the added capacitance will be negligible.

Output Characteristics

The fan-out of the UTILOGIC II AND gate is 10 to standard UTILOGIC II source loads. The AND gate does not have output current sinking capability; therefore, it cannot drive sink loads. The AND gate can drive any of the UTILOGIC II source loads. The AND gate outputs should not be paralleled with the outputs of any other circuits as in collector logic configurations. However, outputs of AND gates may be connected to increase fan-out if the inputs of the two circuits are in common.

Characteristic Curves

The following characteristic curves are normalized, when applicable, to the standard data sheet conditions.

Figure 3 shows the test circuit and definition of T_1 and T_2. The switching times (T_1 and T_2) of the UTILOGIC II AND gates are shown as a function of load capacitance, fan-out, supply voltage, temperature, and load resistance.

The input current versus input voltage relationship shown in Figure 4 is vital at interfaces and also allows computation of margins at non-standard conditions of fan-out.

Offset voltage, which is defined as the input voltage minus the output voltage, is shown in Figure 4F as a function of temperature. Full rated load current is applied to the outputs. Input voltages correspond to worst case UTILOGIC II or Binary Element "1" and "0" output voltage levels.

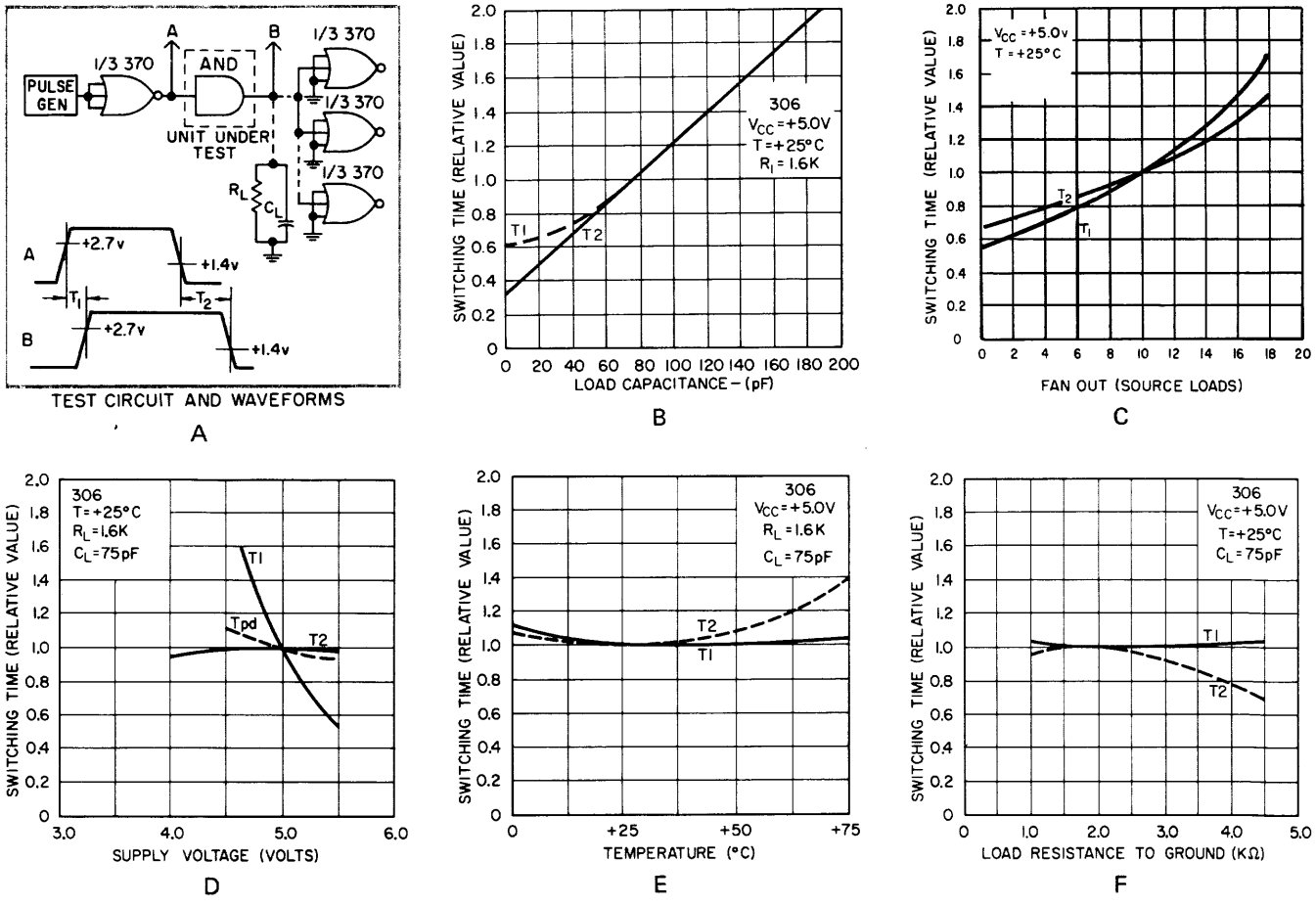


Figure 3 AND Gate Switching Characteristics

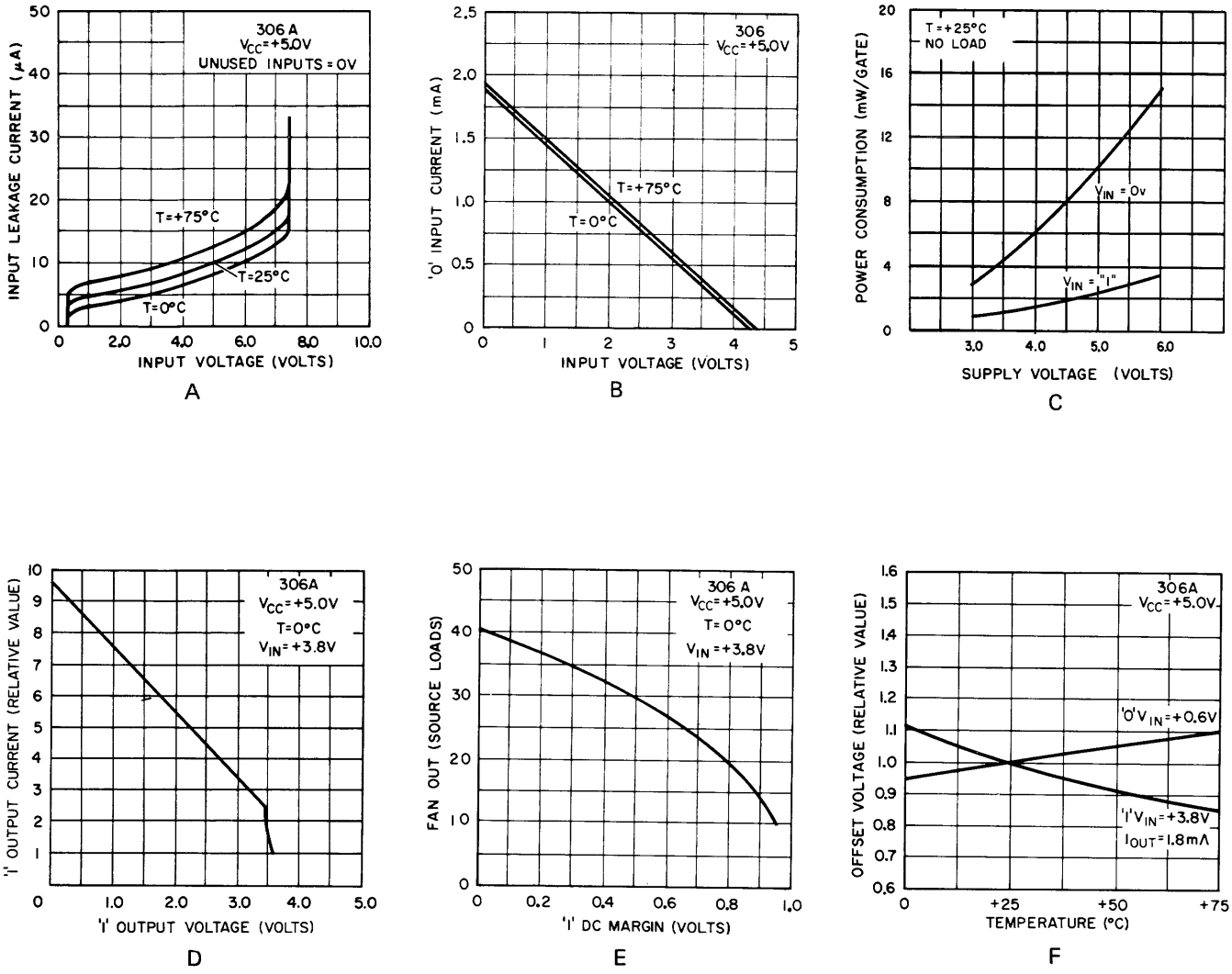


Figure 4 AND Gate DC Characteristics

UTILOGIC II NOR Gates and Expander

The UTILOGIC II NOR gates (314, 370, and 380), Expandable NOR gate (317) and Expander (300), are all derived from the same basic circuit chip to ensure full compatibility of the Expandable Gates and Expander, and to give all the circuits identical electrical characteristics. However, the 300 and 317 will have longer turn-off delay times (T_2) because of the additional capacitive loading on the expansion input. Turn-on delays (T_1) are not sensitive to this capacitance because the source impedance is low during turn-on.

The 300 Expander circuit is characterized in terms of its operation in conjunction with the 317 Expandable NOR and 333 Expandable OR. The ways in which 300 and 317 (as well as 300 and 333) compatibility is guaranteed are of interest. The expansion forward voltage for the 300 and the expansion input voltage of the 317 are measured under the same conditions, and the same limits are guaranteed. In addition, the 300 input leakage current and the 317 "0" input current specifications guarantee reverse current compatibility. These specifications assure the user that the 300 and 317 or the 300 and 333 combination will have the same DC characteristics as when the 317 or 333 is used alone. AC characteristics are shown later (with the 317 and 333 curves) as a function of the capacitance on the expansion input.

CIRCUIT DESCRIPTION

The UTILOGIC II NOR gate (Figures 5, 6, 7, and 8) may be considered as a derivation of the DTL NOR gate. The input diodes of the DTL NOR were replaced with

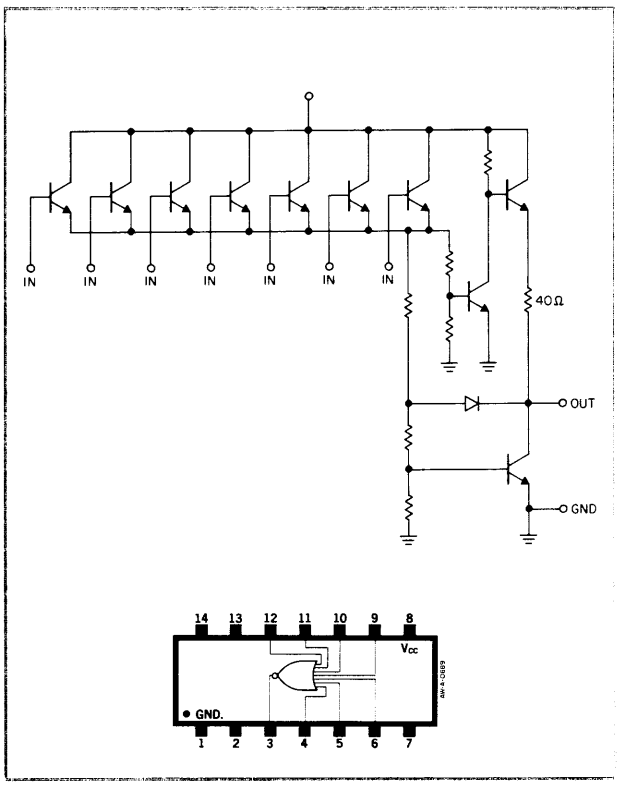


Figure 5 314 7-Input NOR Gate

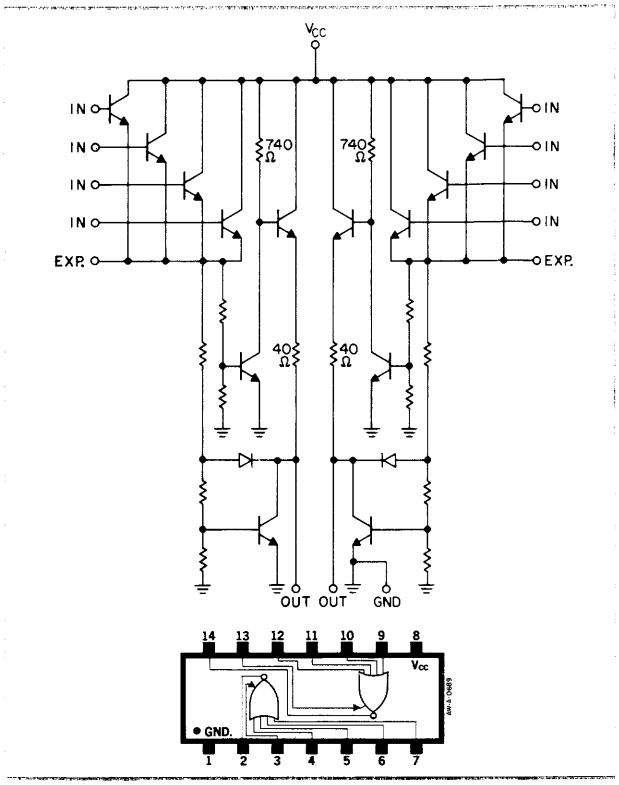


Figure 6 317 Dual 4-Input Expandable NOR Gate

transistors to decrease the input current to allow larger source fan-out capabilities from the NOR and other circuits in the family. The NOR employs a totem-pole output to obtain low output impedance in both the "1" and "0" states. The switching thresholds are determined by the ratio of the coupling resistance to the pull-down resistance at the base of each switching transistor. The series resistor at the output provides current-limiting should the output become accidentally shorted to ground. The Expandable NOR is implemented by connecting the common emitters of the input transistors to an expansion input. The Expander (Figure 9) is a dual array of input transistors; thus, the effect of connecting the Expander output to an expansion input is the same as connecting more input transistors in parallel.

Input Characteristics

The Standard UTILOGIC II Source Load is the NOR input. The Standard Source Load may be simulated by a 10 kΩ resistor and 2 series diodes to ground. An unused NOR input should be tied to ground through a resistance of 60 kΩ (or less) or connected in common with a used input on the same circuit. The capacitance of an open input may become charged during prolonged "1" levels at a driven input. When the driven input goes from "1" to "0", the charged capacitance discharges into the input and gives the effect of a slow circuit. Two or more common inputs represent the same DC load as a single input since the "1" input current is determined by the voltage across the coupling resistors and the gain of the input transistors. Neither of these values changes appreciably when inputs are connected in common. The additional capacitance of a commoned input has no measurable effect on switching times. Input voltages should not exceed the supply voltage unless precautions are taken to limit the resulting current in the collector-base junction of the input transistor to 30 mA.

Output Characteristics

A UTILOGIC II NOR gate has a fan-out of 5 sink loads and 11 source loads. All 16 loads may be connected simultaneously because they do not interact. Because the NOR gates employ transistors for both pull-up and pull-down, their outputs cannot be connected in parallel with the output of any other independent circuit (collector logic). Parallel operation of an active device with another device may result in ambiguous output voltages and/or excessively high currents if one device should attempt to reach a "1" level while the other is attempting to reach a level "0". However, two NORs in the same package may be connected with common inputs and common outputs. In this case, fan-out is doubled and the input loading is two Standard Source Loads.

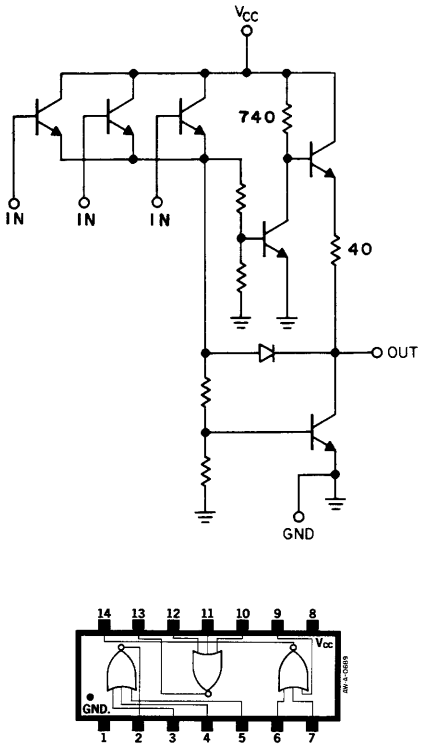


Figure 7 370 Triple 3-Input NOR Gate

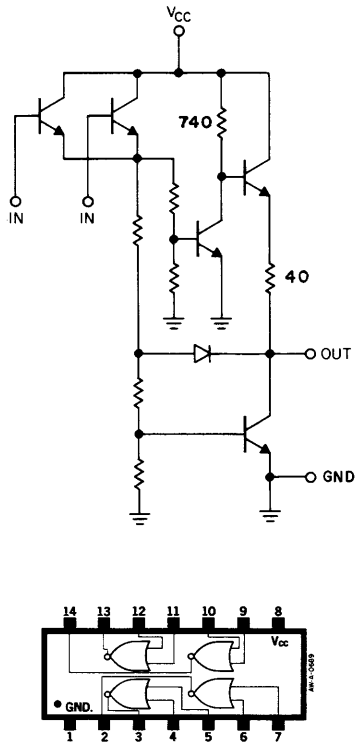


Figure 8 380 Quad 2-Input NOR Gate

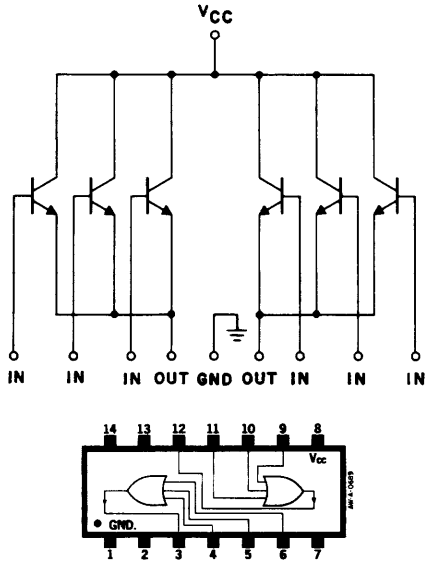
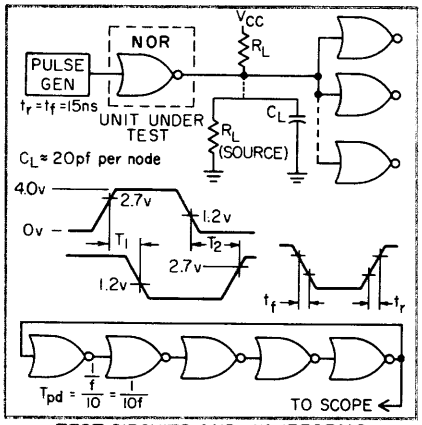
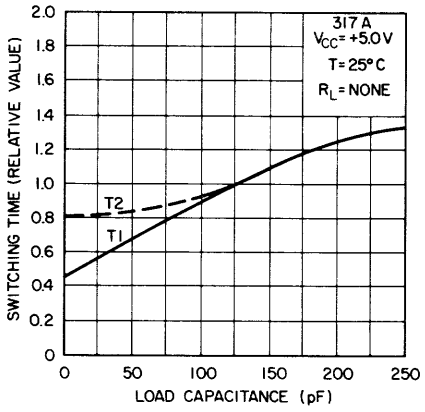


Figure 9 300 Dual 3-Input EXPANDER



TEST CIRCUITS AND WAVEFORMS

A



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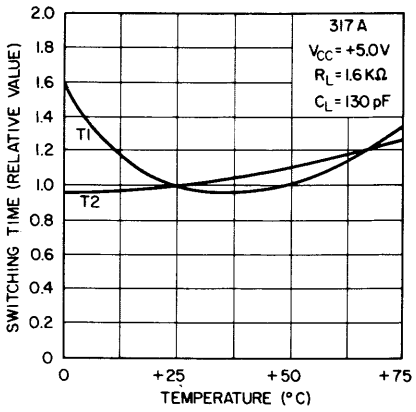
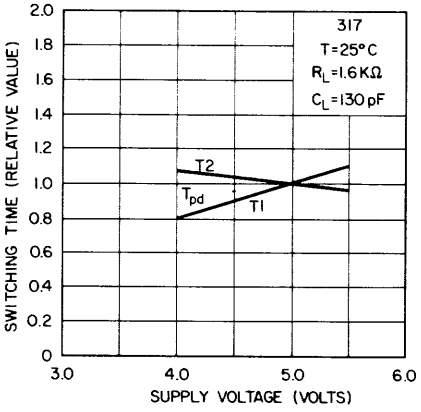
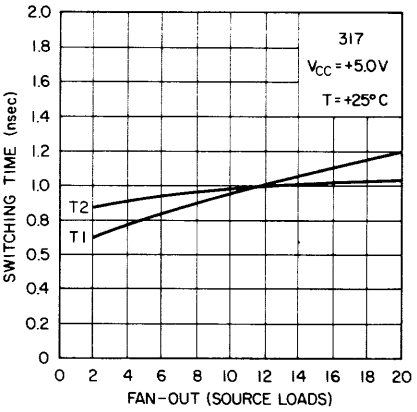


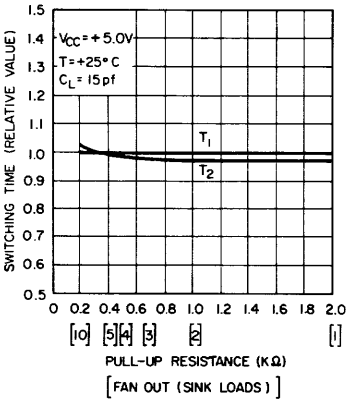
C



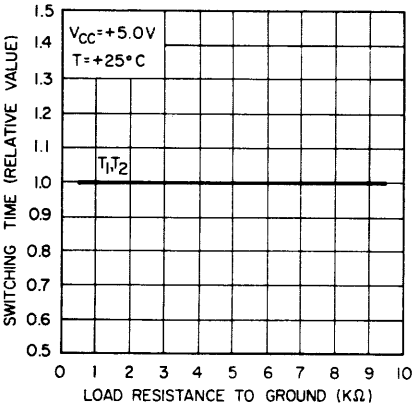
D



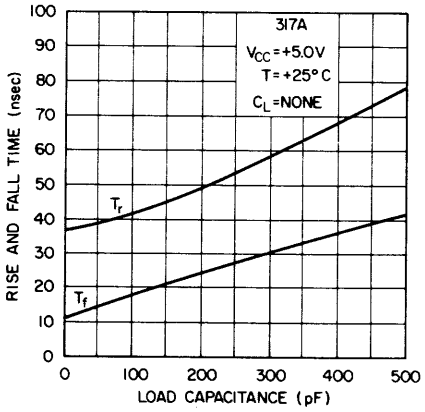
E



F



G



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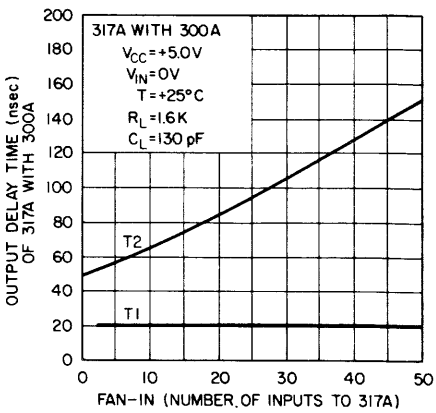

I

Figure 10 NOR Gate Switching Characteristics