SSS725

INSTRUMENTATION OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

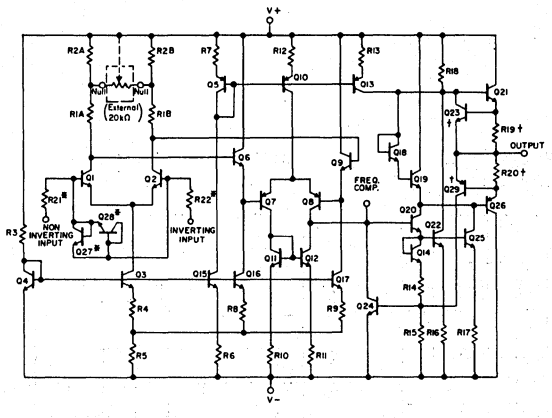
The SSS725 Series of monolithic Instrumentation Operational Amplifiers is specifically designed for accurate high-gain amplification of low level input signals in the presence of large common mode voltages. Superior DC input characteristics include very low offset voltage and current, extremely high open loop gain, low 1/f and wideband noise and a complete absence of "popcorn" noise. The extremely low offset voltage drift is further improved by an advanced nulling technique that provides optimum TCV_{OS} performance when V_{OS} has been nulled to zero. Very high common mode and power supply rejection enable accurate performance in the presence of large spurious signals.

Flexible external compensation provides wide bandwidth and high slew rate operation in high closed-loop gain applications. The superior long term stability, and compatibility with MIL-STD-883 processing make the SSS725 an excellent choice for high reliability process control and aerospace applications, including strain gauge and thermocouple amplifiers, low noise audio amplifiers and instrumentation amplifiers. The SSS725 Series are direct replacements for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short circuit protection**. Further improvements in input performance plus **complete internal frequency compensation** are available: request the OP-05 Instrumentation and OP-07 Ultra-low Offset Voltage Operational Amplifier data sheets.

FEATURES

- **Very High Voltage Gain . . . . . 1000 kV/V Min**
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature (TCV_{OS}). . 0.6 μV/°C Max**
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common Mode Rejection . . . . . 120 dB Min**
- **High Power Supply Rejection . . . . . 2 μV/V Max**
- **Wide Supply Range . . . . . ±1.5V to ±22V**
- **±30V Input Overvoltage Protection**
- **MIL-STD-883 Processing Available**

SIMPLIFIED SCHEMATIC

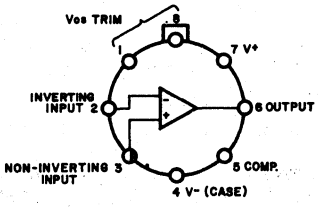


*Q27, Q28, R21, R22 COMPRISE THE INPUT PROTECTION CIRCUIT.

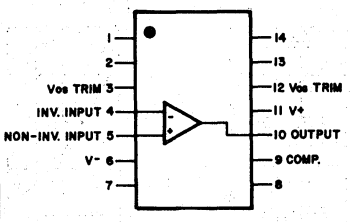
†Q23, Q29, R19, R20 COMPRISE THE OUTPUT PROTECTION CIRCUIT.

PIN CONNECTIONS AND ORDERING INFORMATION

TOP VIEW

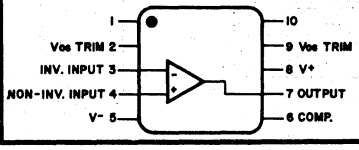


TO-99 (J-Suffix)
ORDER: SSS725AJ
SSS725J
SSS725BJ
SSS725EJ
SSS725CJ



14 PIN DIP (Y-Suffix)*
ORDER: SSS725AY
SSS725Y
SSS725BY
SSS725EY
SSS725CY

*Formerly "P" Suffix



10 PIN FLATPACK
(L-Suffix)
ORDER: SSS725AL
SSS725L
SSS725BL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V	Operating Temperature Range	
Internal Power Dissipation (Note 1)	500mW	SSS725A, SSS725	−55°C to +125°C
Differential Input Voltage	±30V	SSS725B	−25°C to +85°C
Input Voltage (Note 2)	±22V	SSS725E, SSS725C	0°C to +70°C
Output Short Circuit Duration	Indefinite		
Storage Temperature Range	−65°C to +150°C	Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

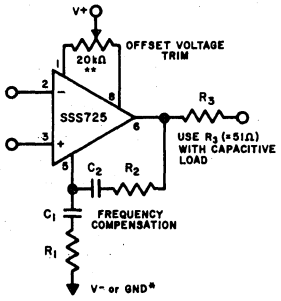
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (J)	80°C	7.1mW/°C
DUAL-IN-LINE (Y)	100°C	10.0mW/°C
FLAT (L)	62°C	5.7mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

FREQUENCY COMPENSATION

COMPENSATION CIRCUIT



COMPENSATION VALUES

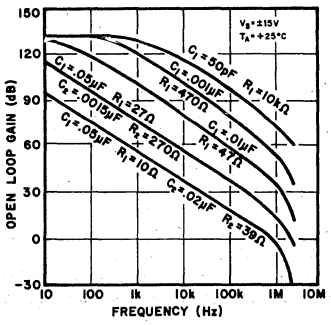
Avcl	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10K	50pF	–	–
1000	470	.001	–	–
100	47	.01	–	–
10	27	.05	270	.0015
1	10	.05	39	.02

*The compensation network (R_1, C_1) should be returned to the V-terminal. If the network is returned to ground, serious degradation of power supply rejection performance with frequency will occur. See typical curves, page 6-49 (PSRR vs FREQUENCY).

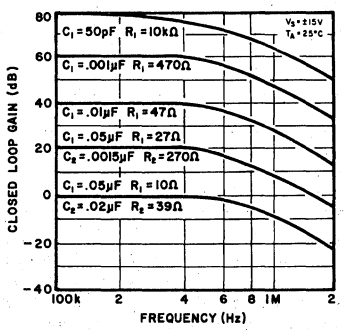
** The trimming potentiometer should be 20KΩ for optimum nulled offset voltage drift. See page 6-49 for change in drift caused by potentiometers ranging from 5KΩ to 100KΩ.

TYPICAL DYNAMIC PERFORMANCE CURVES

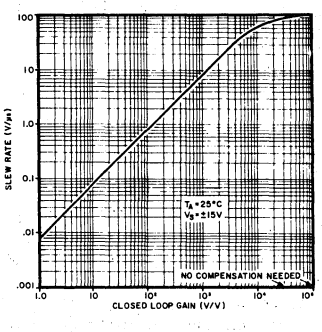
OPEN LOOP RESPONSE FOR VALUES OF COMPENSATION



CLOSED LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



ELECTRICAL CHARACTERISTICS			SSS725E			SSS725C			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	$R_s \leq 20k\Omega$	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{os}		—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 1) f_o = 100Hz (Note 1) f_o = 1000Hz (Note 1)	— — —	9.0 8.0 7.0	15.0 9.0 7.5	— — —	9.0 8.0 7.0	15.0 9.0 7.5	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	fo = 10Hz (Note 1) fo = 100Hz (Note 1) fo = 1000Hz (Note 1)	— — —	0.5 0.25 0.15	1.2 0.6 0.25	— — —	0.6 0.3 0.2	1.4 0.7 0.3	$pA/\sqrt{Hz}$
Input Resistance	R_{in}		0.7	1.8	—	0.5	1.5	—	MΩ
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$ V_O ±10V	1,000,000	3,000,000	—	500,000	3,000,000	—	V/V
Output Voltage Swing	V_{om}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0	±13.0 ±12.8 ±12.5	— — —	±12.0 ±11.5 —	±13.0 ±12.8 ±12.0	— — —	V V V
Input Voltage Range	CMVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common Mode Rejection Ratio	CMRR	$R_s \leq 20k\Omega$	120	126	—	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$R_s \leq 20k\Omega$	—	1.0	5.0	—	2.0	10	μV/V
Power Consumption	P_d		—	90	120	—	110	150	mW
Large Signal Voltage Gain	A_{vo}	$R_L \geq 500\Omega$ V_O ±0.5V V_S ±3V	100,000	600,000	—	60,000	600,000	—	V/V
Power Consumption	P_d	V_S ±3V	—	4	6	—	4	8	mW
The following specifications apply for V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.									
Input Offset Voltage (Without external trim)	V_{os}	$R_s \leq 20k\Omega$	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (without external trim)	TCV_{os}	R_s 50Ω (Note 2)	—	0.7	2.0 (Note 1)	—	1.4	4.5 (Note 1)	μV/°C
Average Input Offset Voltage Drift (with external trim)	TCV_{osn}	R_s 50Ω (Note 2)	—	0.2	0.6	—	0.5	1.5 (Note 1)	μV/°C
Input Offset Current	I_{os}	T_A MAX T_A MIN	— —	0.65 0.9	5.0 7.0	— —	2.0 3.0	15 25	nA nA
Average Input Offset Current Drift	TCI_{os}		— —	4	40 (Note 1)	— —	14	150 (Note 1)	pA/°C
Input Bias Current	I_B	T_A MAX T_A MIN	— —	30 35	80 100	— —	35 45	110 180	nA nA
Common Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$	115	118	—	97	113	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$	—	1.5	7.0	—	3.0	15	μV/V
Large Signal Voltage Gain	A_{vo}	V_O ±10V; R_L>2kΩ T_AMAX T_AMIN	1,000,000 800,000	3,200,000 2,700,000	— —	400,000 300,000	3,200,000 2,700,000	— —	V/V
Maximum Output Voltage Swing	V_{om}	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

Note 1: Parameter is not 100% tested. 90% of all units meet these specifications.

Note 2: Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.